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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/388,766	09/02/1999	BOHR-WINN SHIH	303.513US1	4410

21186 7590 01/09/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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MINNEAPOLIS, MN 55402

EXAMINER

SHARON, AYAL I

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 01/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



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DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

09/388,766

Applicant(s)

SHIH ET AL.

Examin r

Ayal I Sharon

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Introduction

1. Claims 1-35 of U.S. Application 09/388,766, originally filed on 09/02/1999, have been amended in an RCE filed on 9/22/03. New art has been applied in the claim rejections.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office Action:

A person shall be entitled to a patent unless-

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The prior art cited is as follows:
4. IEEE Std 1364-1995. IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language. Copyright 1995. (Henceforth referred to as "**IEEE 1364**". Sections 1,3,6,7,9,12,14,18,19,22, pp. i-ix, and the Index of this 675 page reference have included in the file wrapper and have been provided to the Applicants. The entire reference will be provided to the Applicants upon request.).

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5. The claims are subsequently recited for Applicant's convenience. Applicant's attention is also directed to the pertinent sections of the prior art.

6. Claims 1-8, 12-30, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by IEEE 1364.

7. IEEE 1364 teaches the limitations of Claim 1:

1. (Currently Amended) A method of simulating a node using a simulation program that includes multiple, linked modules, the method comprising:

executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13; Section 6, pp.50-52;)

simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the functions of
(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-106)

forcing an initial forced logic state on the node;
(See IEEE 1364, especially: Section 9, pp.104-106)

releasing the node from the forced logic state if a predetermined condition is met, which enables the simulation program to change a logic state of the node
(See IEEE 1364, especially: Section 9, pp.104-106)

monitoring the released node after the node has been released; and
(See IEEE 1364, especially: Section 9, pp.104-106; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

providing an indication, in response to the monitoring, when the node is in a pre-selected condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

8. IEEE 1364 teaches the limitations of Claim 2:

2. (Currently Amended) The method of claim 1, wherein forcing the initial forced logic state includes forcing to a logic zero, logic one or high-impedance.
(See IEEE 1364, especially: Section 3, p.13)

9. IEEE 1364 teaches the limitations of Claim 3:

3. (Original) The method of claim 1, wherein releasing the node further comprises determining that the condition is met after passage of a predetermined amount of time.

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(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119; Section 14, pp.187-196; Section 18, pp.234, 246-247;)

10. IEEE 1364 teaches the limitations of Claim 4:

4. (Currently Amended) The method of claim 3, wherein releasing the node further comprises determining that the condition is met when the node has been resolved.
(See IEEE 1364, especially: Section 3, p.17-19)

11. IEEE 1364 teaches the limitations of Claim 5:

5. (Currently Amended) The method of claim 1, wherein providing an indication includes indicating when the released node is in an unknown logic state.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247; Section 3, p.13)

12. IEEE 1364 teaches the limitations of Claim 6:

6. (Currently amended) The method of claim 1, further comprising providing an error indication when the release node is in a pre-selected condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

13. IEEE 1364 teaches the limitations of Claim 7:

7. (Original) The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119; Section 14, pp.187-196; Section 18, pp.234, 246-247;)

14. IEEE 1364 teaches the limitations of Claim 8:

8. (Currently Amended) A method of initializing and monitoring a simulated circuit node using a simulation program that includes multiple linked modules, the method comprising:

executing a first circuit module that simulates a circuit having a node, wherein the node represents -a simulated electrical connection point of the circuit;
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13; Section 6, pp.50-52;)

simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the functions of
(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-106)

obtaining an initial node condition for the node, wherein the initial node condition is a logic state;
(See IEEE 1364, especially: Section 14, pp.179-180; Section 18, pp.234, 246-247;)

forcing the node to the initial node condition;
(See IEEE 1364, especially: Section 9, pp.104-106)

testing the node for a valid condition;
(See IEEE 1364, especially: Section 9, pp.106-107)

monitoring the node; and
(See IEEE 1364, especially: Section 14, pp.179-180; Section 18, pp.234, 246-247;)

providing an indication when the node is in an undesirable condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

15. IEEE 1364 teaches the limitations of Claim 12:

12. (Original) The method of claim 8, further comprising outputting the condition of the simulated node.
(See IEEE 1364, especially: Section 9, p.110; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

16. IEEE 1364 teaches the limitations of Claim 13:

13. (Original) The method of claim 8, further comprising obtaining a simulation run time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119; Section 14, pp.183-196, 202-204; Section 18, pp.234, 246-247;)

17. IEEE 1364 teaches the limitations of Claim 14:

14. (Original) The method of claim 13, further comprising outputting a final node condition when the simulation run time is completed.
(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

18. IEEE 1364 teaches the limitations of Claim 15:

15. (Currently Amended) A computer-readable medium having computer-executable instructions comprising:

at least one selectable circuit module, which when executed simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit; and
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13; Section 6, pp.50-52;)

at least one selectable behavior module, which is linkable to a circuit module, and which when executed results in

(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-106)

forcing an initial forced logic state on the node;

(See IEEE 1364, especially: Section 9, pp.104-106)

releasing the node from the forced logic state if a predetermined condition is met, which enables a simulation program to change a logic state of the node and

(See IEEE 1364, especially: Section 9, pp.104-106)

monitoring the node after the node has been released; and

(See IEEE 1364, especially: Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

providing an indication, in response to the monitoring, when the node is in a preselected condition.

(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

19. IEEE 1364 teaches the limitations of Claim 16:

16. (Currently Amended) The medium of claim 15, having further computer-executable instructions for forcing the initial forced logic state to a logic zero, logic one or high-impedance.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.104-106)

20. IEEE 1364 teaches the limitations of Claim 17:

17. (Original) The medium of claim 15, having further computer-executable instructions for determining that the condition is met after passage of a predetermined amount of time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119;
Section 14, pp.179-190, 183-196, 202-204; Section 18, pp.234, 246-247;)

21. IEEE 1364 teaches the limitations of Claim 18:

18. (Currently Amended) The medium of claim 15, having further computer-executable instructions for determining that the condition is met when the node a valid logic value.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.106-113)

22. IEEE 1364 teaches the limitations of Claim 19:

19. (Currently amended) The medium of claim 18, having further computer-executable instructions for indicating when the release node is in an unknown logic state.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.104-106;
Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

23. IEEE 1364 teaches the limitations of Claim 20:

20. (Currently Amended) A simulation module of a simulation program, the simulation

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module comprising:

an input means for inputting an initial node condition into a simulated circuit node of a circuit module linked with the simulation module, wherein the simulated circuit node represents a simulated electrical connection point of the circuit module;

(See IEEE 1364, especially: Section 3, p.13; Section 6, pp.50-52; Section 9, pp.104-106; Section 12, pp.135-139;)

a conveying means for conveying the initial node condition to the simulated circuit node;

(See IEEE 1364, especially: Section 9, pp.104-106;)

release means for releasing the simulated circuit node from the initial node condition upon satisfaction of a condition, wherein releasing the simulated circuit node enables the simulation program to change a logic state of the simulated circuit node;

(See IEEE 1364, especially: Section 9, pp.104-106;)

a monitoring means for monitoring the simulated circuit node for a node condition; and

(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

an output means, responsive to the monitoring means, for outputting an indication when the node condition is in an undesirable state.

(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

24. IEEE 1364 teaches the limitations of Claim 21:

21. (Original) The module of claim 20, further comprising an output means for outputting the node condition.

(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

25. IEEE 1364 teaches the limitations of Claim 22:

22. (Original) The module of claim 20, further comprising an input means for inputting a simulation run time.

(See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107 and pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18, pp.234, 246-247;)

26. IEEE 1364 teaches the limitations of Claim 23:

23. (Original) The module of claim 22, further comprising an output means for outputting a final node condition at completion of the simulation run time.

(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

27. IEEE 1364 teaches the limitations of Claim 24:

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24. (Currently Amended) A computerized system for initializing and monitoring a simulated circuit node, the system comprising:

a circuit simulation tool;
(See IEEE 1364, especially: Section 1.2)

at least one selectable circuit module, which when executed simulates a circuit having the simulated circuit node, wherein the simulated circuit node represents a simulated electrical connection point of the circuit; and

(See IEEE 1364, especially: Section 12, pp.135-139)

at least one selectable behavior module, which is linkable to a circuit module, and which includes

(See IEEE 1364, especially: Section 9, pp.98-99)

a first input means for inputting an initial node condition;
(See IEEE 1364, especially: Section 9, pp.104-106)

a conveying means for conveying the initial node condition to the simulated circuit node;

(See IEEE 1364, especially: Section 9, pp.104-106)

a release means for releasing the initial node condition, wherein releasing the initial node condition enables the circuit simulation tool to change a logic state of the simulated circuit node;

(See IEEE 1364, especially: Section 9, pp.104-106)

a monitoring means for monitoring the simulated circuit node for a node condition;
(See IEEE 1364, especially: Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

a first output means for outputting an indication when the node condition is in an undesirable state;

(See IEEE 1364, especially: Section 9, pp.110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

a second input means for inputting a simulation run time; and
(See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107 and
pp.114-119; Section 14, pp.179-190, 183-196, 202-204;
Section 18, pp.234, 246-247;)

a second output means for outputting a final node condition at completion of the simulation run time.

(See IEEE 1364, especially: Section 9, pp.110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

28. IEEE 1364 teaches the limitations of Claim 25:

25. (Currently Amended) An HDL initial condition module comprising:

a means for maintaining a logic level of a simulated circuit node until a release condition is met, wherein

(See IEEE 1364, especially: Section 9, pp.104-106)

the simulated circuit node represents a simulated electrical connection point of a simulated circuit and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module, and

(See IEEE 1364, especially: Section 3, pp.13-16; Section 12, pp.135-139;)

a simulation program is able to change a logic state of the simulated circuit node after the release condition is met.

(See IEEE 1364, especially: Section 9, pp.104-106)

29. IEEE 1364 teaches the limitations of Claim 26:

26. (Currently Amended) The module of claim 25 wherein the release condition is when a known logic state can be determined for the simulated circuit node.

(See IEEE 1364, especially: Section 9, pp.104-106, 110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

30. IEEE 1364 teaches the limitations of Claim 27:

27. (Original) The module of claim 25 wherein the logic level is a value defined by an HDL executable simulation program.

(See IEEE 1364, especially: Section 9, pp.104-106)

31. IEEE 1364 teaches the limitations of Claim 28:

28. (Currently Amended) An HDL initial condition module comprising:

an initial condition release means, which enables a simulation program to change a logic state of a simulated circuit node after a release condition is met, wherein the simulated circuit node represents a simulated electrical connection point of a simulated circuit, and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module; and

(See IEEE 1364, especially: Section 3, pp.13-16; Section 9, pp.104-106, 110-111; Section 12, pp.135-139; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

a simulated circuit node error detection means, which monitors the simulated circuit node for a node condition.

(See IEEE 1364, especially: Section 9, pp.104-106, 110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

32. IEEE 1364 teaches the limitations of Claim 29:

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29. (Currently Amended) An HDL initial condition module comprising:

means for maintaining a logic level of a simulated circuit node for a predetermined period of time, wherein the simulated circuit node represents a simulated electrical connection point of a simulated circuit, and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module; and

(See IEEE 1364, especially: Section 3, pp.13-16; Sections 9.2, 9.3, pp.103-107, 110-111, 114-119; Section 12, pp.135-139; Section 14, pp.179-196, 202-204; Section 18, pp.234, 246-247;)

means for releasing an initial condition after a release condition is met, wherein releasing the initial condition enables a simulation program to change the logic level of the simulated circuit node, and wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.

(See IEEE 1364, especially: Sections 9.2, 9.3, pp.99-104, and 106-107 and pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18, pp.234, 246-247;)

33. IEEE 1364 teaches the limitations of Claim 30:

30. (Original) The module of claim 29, wherein the predetermined period of time is a user-defined period of time.

(See IEEE 1364, especially: Section 9, pp.99-104, 106-107 and pp.114-119; Section 14.3, 14.5, 14.8; Section 18, pp.234, 246-247;)

34. In regards to Claim 33, IEEE 1364 teaches a simulated HDL circuit device

(Section 1, pp. iii-iv, 1-4), a plurality of HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), behavior modules (Section 9), assigning/de-assigning and forcing/releasing node values, and condition statements (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), and outputting an undesirable state (Section 9, p.111).

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35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

36. The prior art cited is as follows:

37. IEEE Std 1364-1995. IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language. Copyright 1995. (Henceforth referred to as "**IEEE 1364**". Sections 1,3,6,7,9,12,14,18,19,22, pp. i-ix, and the Index of this 675 page reference have included in the file wrapper and have been provided to the Applicants. The entire reference will be provided to the Applicants upon request.).

38. The claims are subsequently recited for Applicant's convenience. Applicant's attention is also directed to the pertinent sections of the prior art.

39. Claims 9-11, 31-32, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE in view of Official Notice.

40. In regards to Claim 9, IEEE 1364 teaches the functionalities of the unknown state (Section 3, p.1), monitoring the state (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), looping statements with conditions (Section 9, pp.111-114), and forcing nodes (Section 9, pp.104-106).

However, IEEE 1364 does not expressly teach the limitations of Claim 9:

9. (Currently Amended) The method of claim 8, wherein the initial node condition is forced again if the testing indicates that the node has an unknown logic value.

Combining the features taught by IEEE 1364 in the configuration claimed by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above to as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value.

41. In regards to Claim 10, IEEE 1364 teaches the functionalities of the unknown and valid logic states (Section 3, p.1), monitoring the state (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), looping statements with conditions (Section 9, pp.111-114), and forcing nodes (Section 9, pp.104-106).

However, IEEE 1364 does not expressly teach the limitations of Claim 10:

10. (Currently Amended) The method of claim 9, wherein the initial node condition is forced and simulation is repeated until the node has a valid logic value.

Combining the features taught by IEEE 1364 in the configuration claimed by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above to as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value. Moreover, it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value.

42. In regards to Claim 11, IEEE 1364 teaches the functionalities of the unknown and valid logic states (Section 3, p.1), monitoring the state (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), looping statements with conditions (Section 9, pp.111-114), and forcing nodes (Section 9, pp.104-106).

However, IEEE 1364 does not expressly teach the limitations of Claim 11:

11. (Currently Amended) The method of claim 10, wherein monitoring only occurs after the node has a valid logic value.

Combining the features taught by IEEE 1364 in the configuration claimed by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above to as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value. Moreover, it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value.

43. In regards to Claim 31, IEEE 1364 teaches a simulated HDL circuit device (Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), assigning/forcing node values, and condition statements (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), and outputting an undesirable state (Section 9, p.111).

IEEE 1364, however, does not expressly teach the use of exactly two modules. (Section 12 enables the implementation of an undefined number of modules). Moreover, IEEE 1364 does not expressly teach that the commands for assigning, monitoring, or outputting node values are implemented as “sub-modules”. Finally, IEEE 1364 does not expressly teach the following limitation:

a second output submodule outputting a second indication when the second node condition is in an undesirable state; and wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

In regards to the use of exactly two modules, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only two components of interest.

In regards to referring to commands for assigning, monitoring, or outputting node values are implemented as “sub-modules”, Examiner interprets Applicant’s use of the term “sub-module” as being functionally equivalent to what is commonly known in the art under the following names: command, function, sub-routine.

Finally, in regards to the first module conveying the initial code condition to the second module (which had an undesirable state), Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit.

44. In regards to Claim 32, IEEE 1364 teaches a simulated HDL circuit device (Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), assigning/de-assigning and forcing/releasing node values, and condition statements (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), and outputting an undesirable state (Section 9, p.111).

IEEE 1364, however, does not expressly teach the use of exactly three modules. (Section 12 enables the implementation of an undefined number of modules). In addition, IEEE 1364 does not expressly teach the following limitation:

a third HDL module, linked to the circuit HDL module, the third HDL module including

a release condition means for releasing the second simulated node on a release condition, wherein releasing the second simulated node enables a simulation program to change a logic level of the second simulated node.

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

In regards to the use of exactly three modules, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only three components of interest.

In addition, in regards to the first module conveying the initial code condition to the second module (which had a released, and therefore changeable, state), Official Notice is given that it would have been obvious to one

of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit.

45. In regards to Claim 34, IEEE 1364 teaches the functionalities of a simulated HDL circuit device (Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), unknown and valid logic states (Section 3, p.1), assigning/de-assigning and forcing/releasing node values (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), outputting an undesirable state (Section 9, p.111), condition statements (Section 9, pp.106-107), and looping statements with conditions (Section 9, pp.111-114)

However, IEEE 1364 does not expressly teach that a simulation is repeated ("continuing in phase one") until the node has a valid logic value.

Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above to as to enable repeatedly re-forcing and then re-releasing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value. Moreover, it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value. In addition, it sometimes takes time for a circuit to get defined inputs from its input circuits.

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46. IEEE 1364 teaches the limitations of Claim 35:

35. (Original) The method of claim 34, wherein simulation completion is a user defined time period.

(See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107 and pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18, pp.234, 246-247;)

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

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Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

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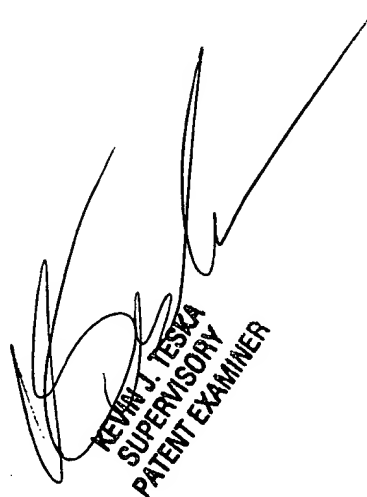
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Any inquiry of a general nature or relating to the status of this application
or proceeding should be directed to the receptionist, whose telephone number is:
(703) 305-3900.

Ayal I. Sharon

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November 22, 2003



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